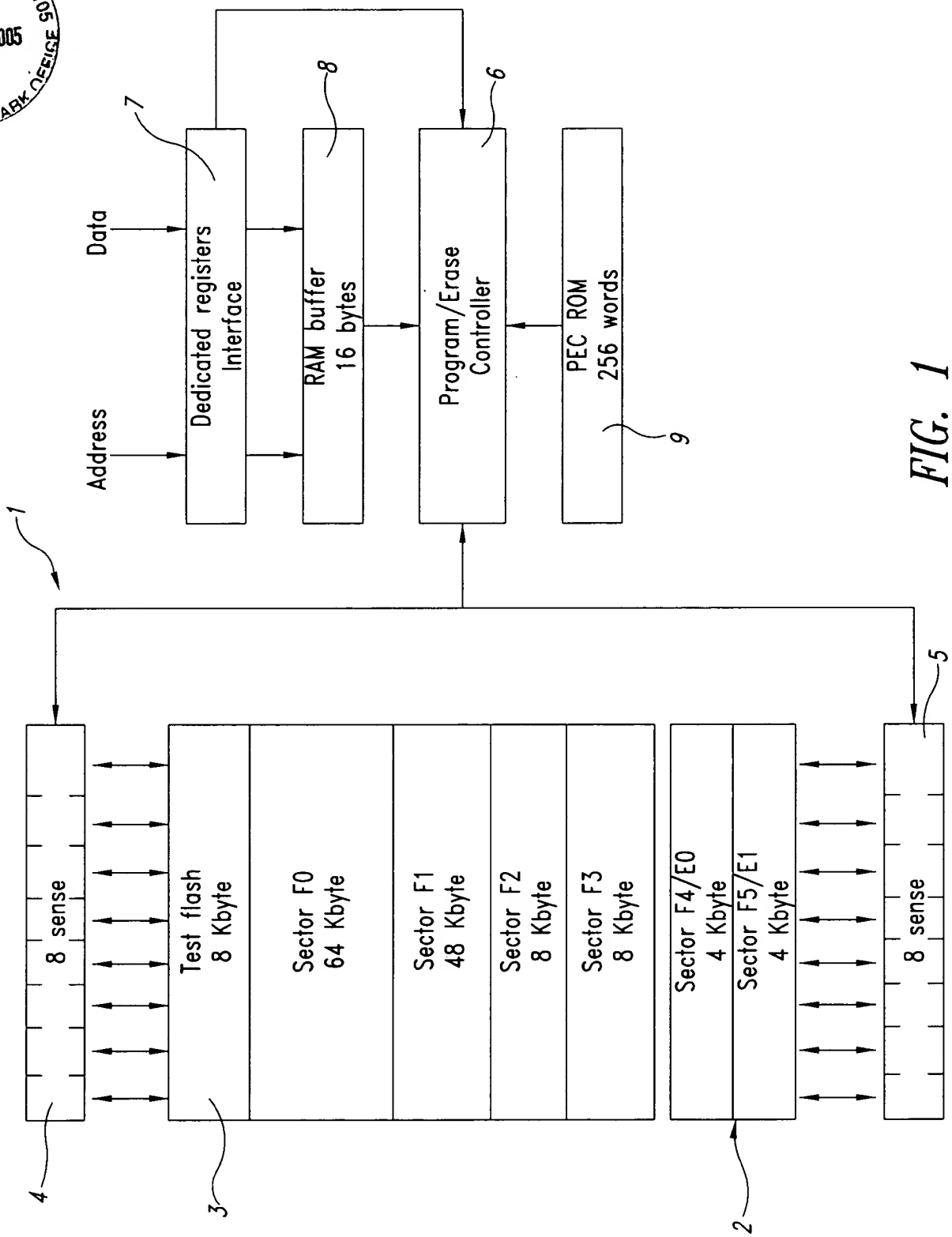


FIG. 1

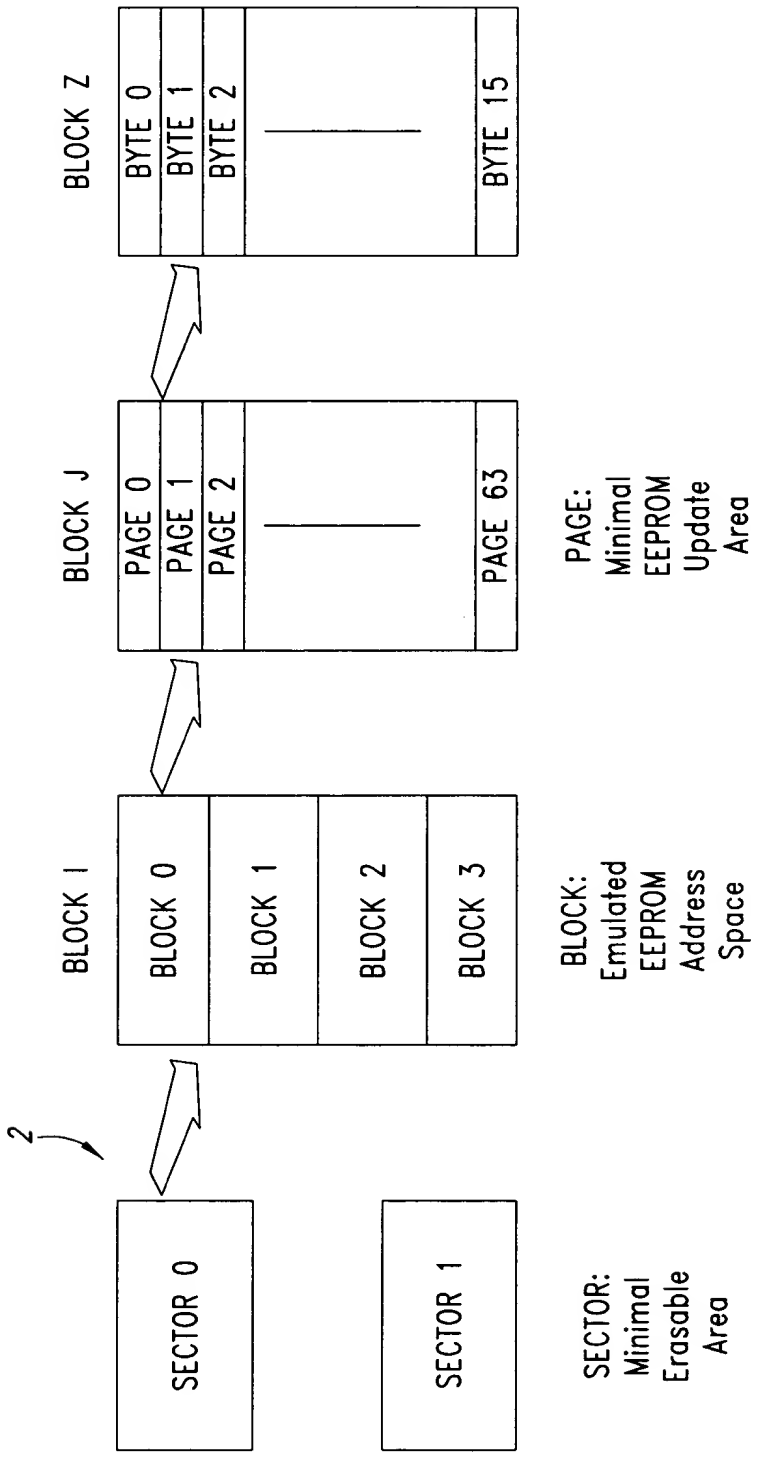
2
SECTOR 0
SECTOR 1
SECTOR: Minimal Erasable Area
BLOCK 0
BLOCK 1
BLOCK 2
BLOCK 3
BLOCK: Emulated EEPROM Address Space
BLOCK I
PAGE 0
PAGE 1
PAGE 2
PAGE 63
PAGE: Minimal EEPROM Update Area
BLOCK J
BYTE 0
BYTE 1
BYTE 2
BYTE 15
BLOCK Z

*FIG. 2*

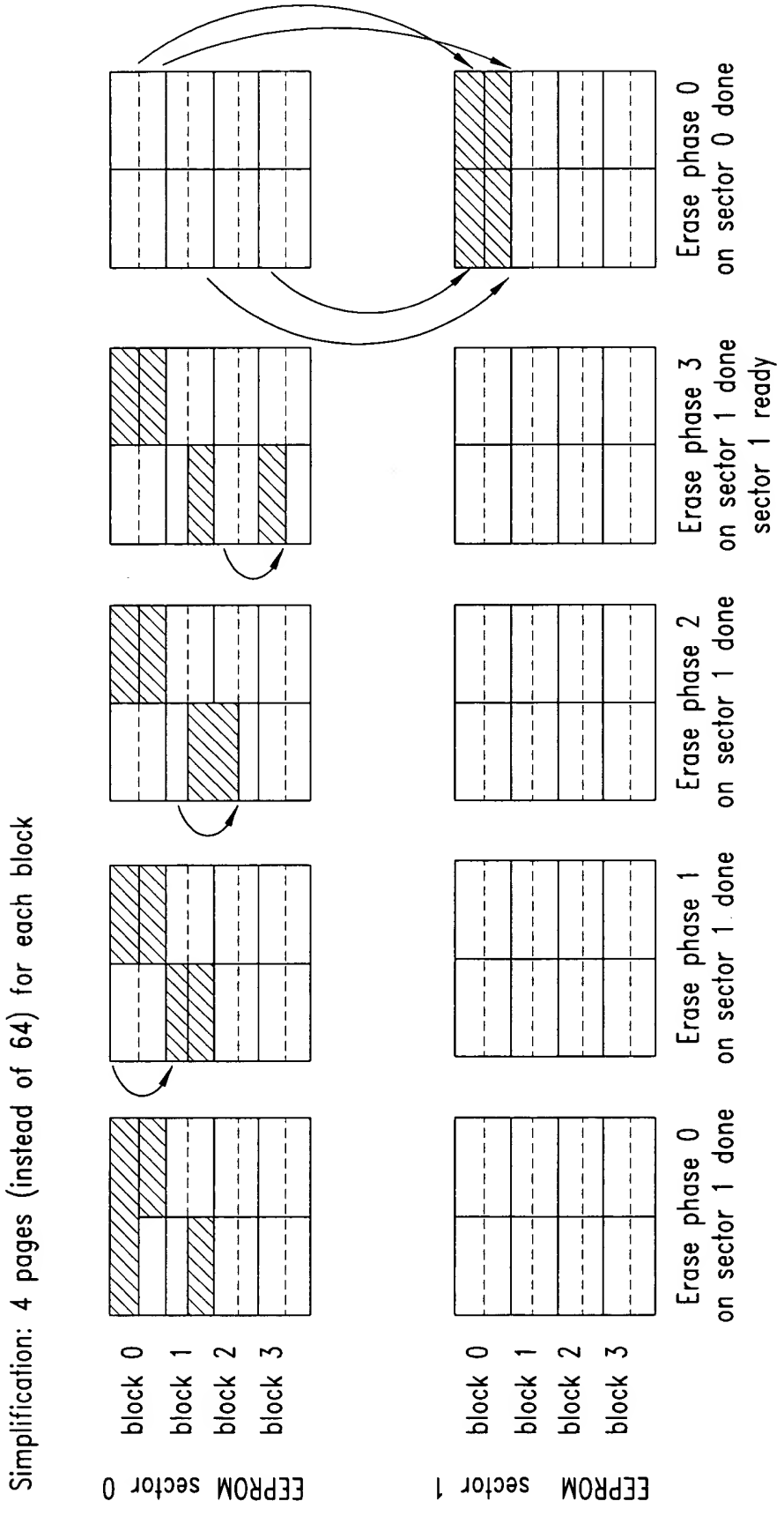
Simplification: 4 pages (instead of 64) for each block
EEPROM sector 0
block 0
block 1
block 2
block 3
EEPROM sector 1
block 0
block 1
block 2
block 3
Erase phase 0 on sector 1 done
Erase phase 1 on sector 1 done
Erase phase 2 on sector 1 done
Erase phase 3 on sector 1 done sector 1 ready
Erase phase 0 on sector 0 done

*FIG. 3*

| | |
|---|---|
| 224000h | FCR |
| 224001h | ECR |
| 224002h | FSR |

*FIG. 3A*

| Sector | Addresses | Max Size |
|---|---|---|
| OTP | 211F80h to 211FFFh | 128 byte |
| Flash 0 | 000000h to 00FFFFh | 64 Kbyte |
| Flash 1 | 01000h to 01BFFFh | 48 Kbyte |
| Flash 2 | 01C000h to 01DFFFh | 8 Kbyte |
| Flash 3 | 01E000h to 01FFFFh | 8 Kbyte |
| EEprom | 220000h to 2203FFh | 1 Kbyte |

*FIG. 3B*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FWMS | FPAGE | FCHIP | FBYTE | FSECT | FSUSP | PROT | FBUSY |

*FIG. 3C*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EWMS | EPAGE | ECHIP | | | WFIS | FEIEN | EBUSY |

*FIG. 3D*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FERR | FSS6 | FSS5 | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 |

*FIG. 3E*

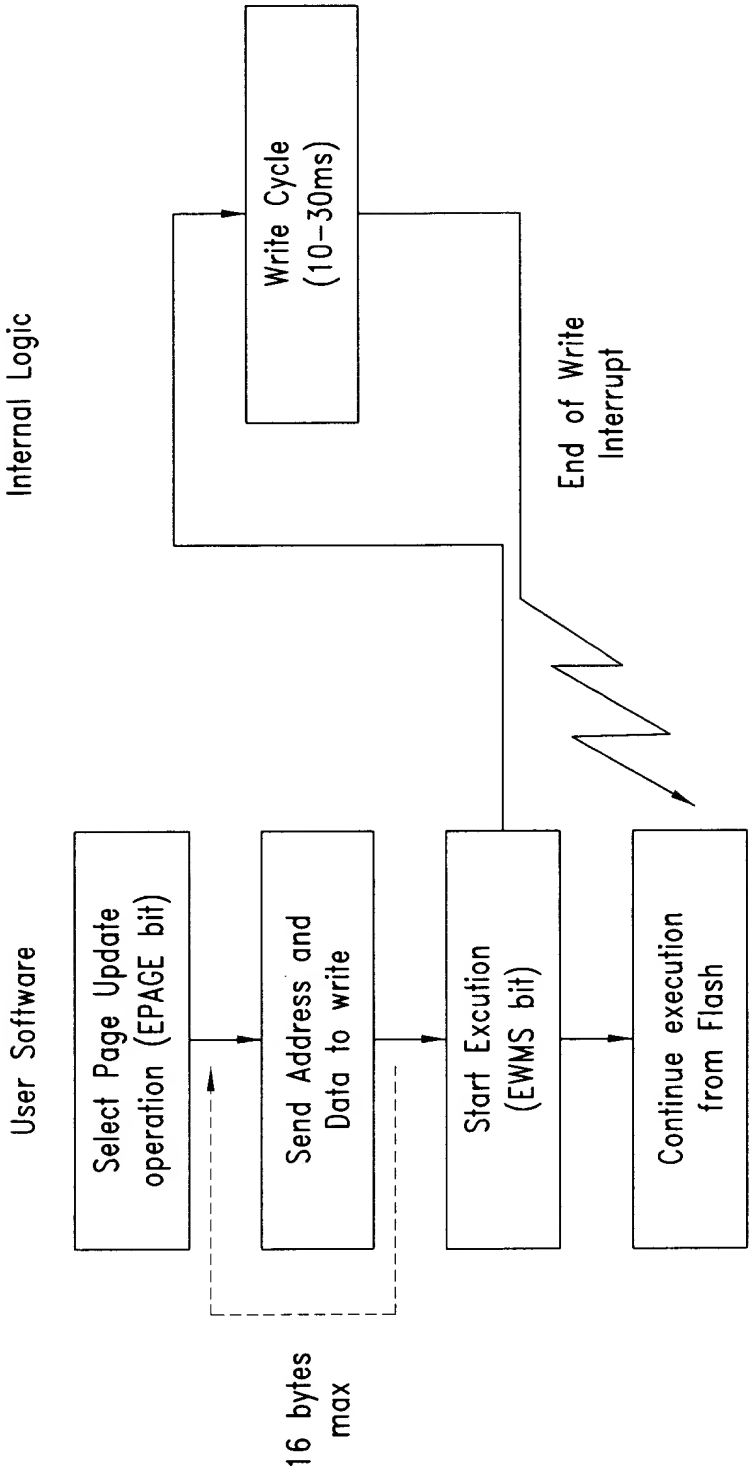
Internal Logic
Write Cycle
(10–30ms)
End of Write
Interrupt
User Software
Select Page Update
operation (EPAGE bit)
Send Address and
Data to write
Start Excution
(EWMS bit)
Continue execution
from Flash
16 bytes
max

*FIG. 4*

| | |
|---|---|
| 211FFCh | NVAPR |
| 211FFDh | NVWPR |
| 211FFEh | NVPWD0 |
| 211FFFh | NVPWD1 |

*FIG. 4A*

| Operation | Size | Min | Typ | Max |
|---|---|---|---|---|
| Page Update | 256 byte | 160 us | 10 ms | 30 ms |
| | 512 byte | 160 us | 15 ms | 50 ms |
| | 1 Kbyte | 160 us | 30ms | 100 ms |
| Chip Erase | 256 byte | | 35 ms | 100 ms |
| | 512 byte | | 45 ms | 150 ms |
| | 1 Kbyte | | 70 ms | 300 ms |

*FIG. 4B*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| APRA | APRO | APBR | APEE | APEX | PWT2 | PWT1 | PWT0 |

*FIG. 4C*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TMDIS | PWOK | WPBR | WPEE | WPRS3 | WPRS2 | WPRS1 | WPRS0 |

*FIG. 4D*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWD7 | PWD6 | PWD5 | PWD4 | PWD3 | PWD2 | PWD1 | PWD0 |

*FIG. 4E*

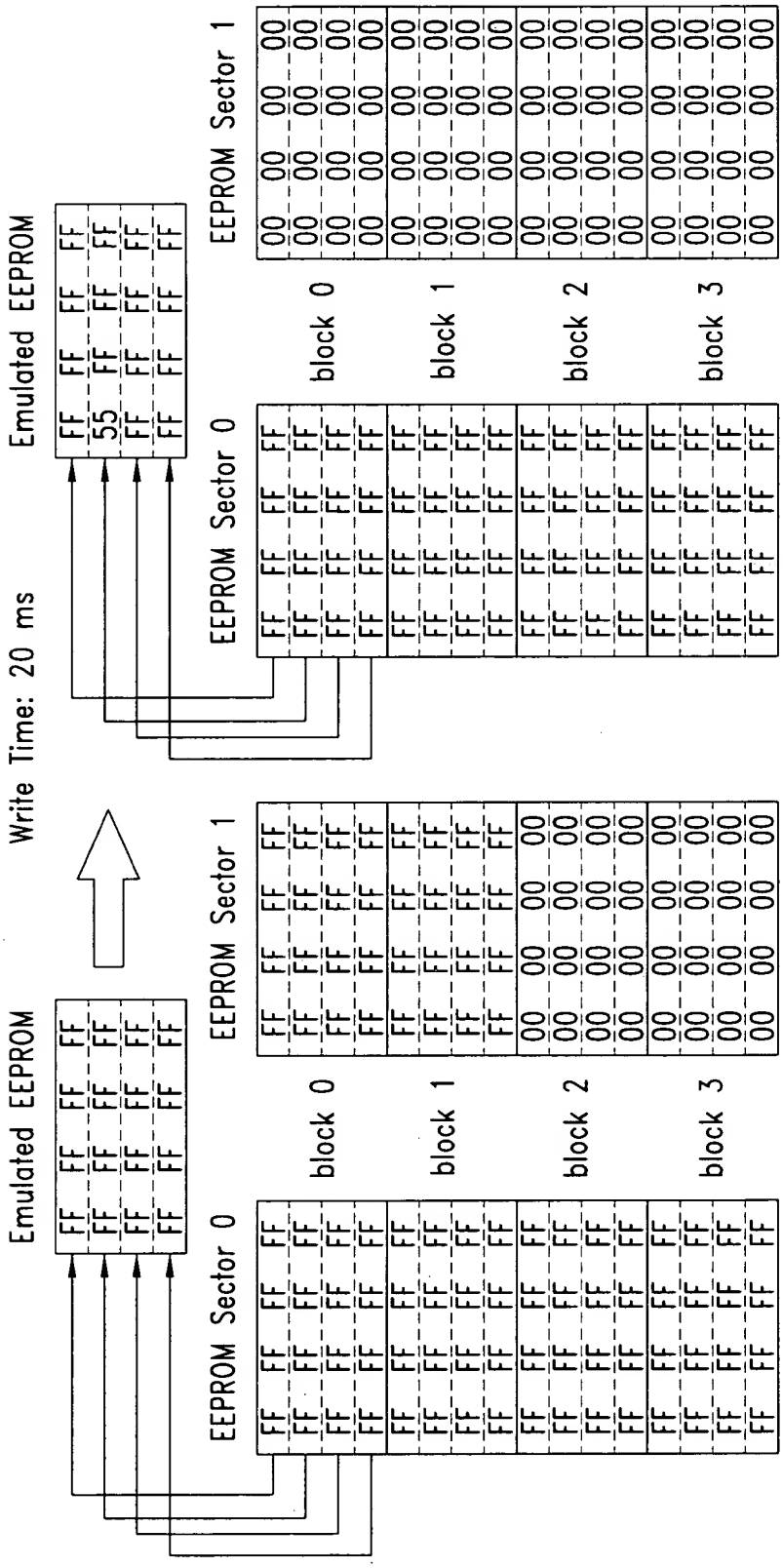
Emulated EEPROM
Write Time: 20 ms
Emulated EEPROM
EEPROM Sector 0
EEPROM Sector 1
block 0
block 1
block 2
block 3
EEPROM Sector 0
EEPROM Sector 1
block 0
block 1
block 2
block 3

*FIG. 5*

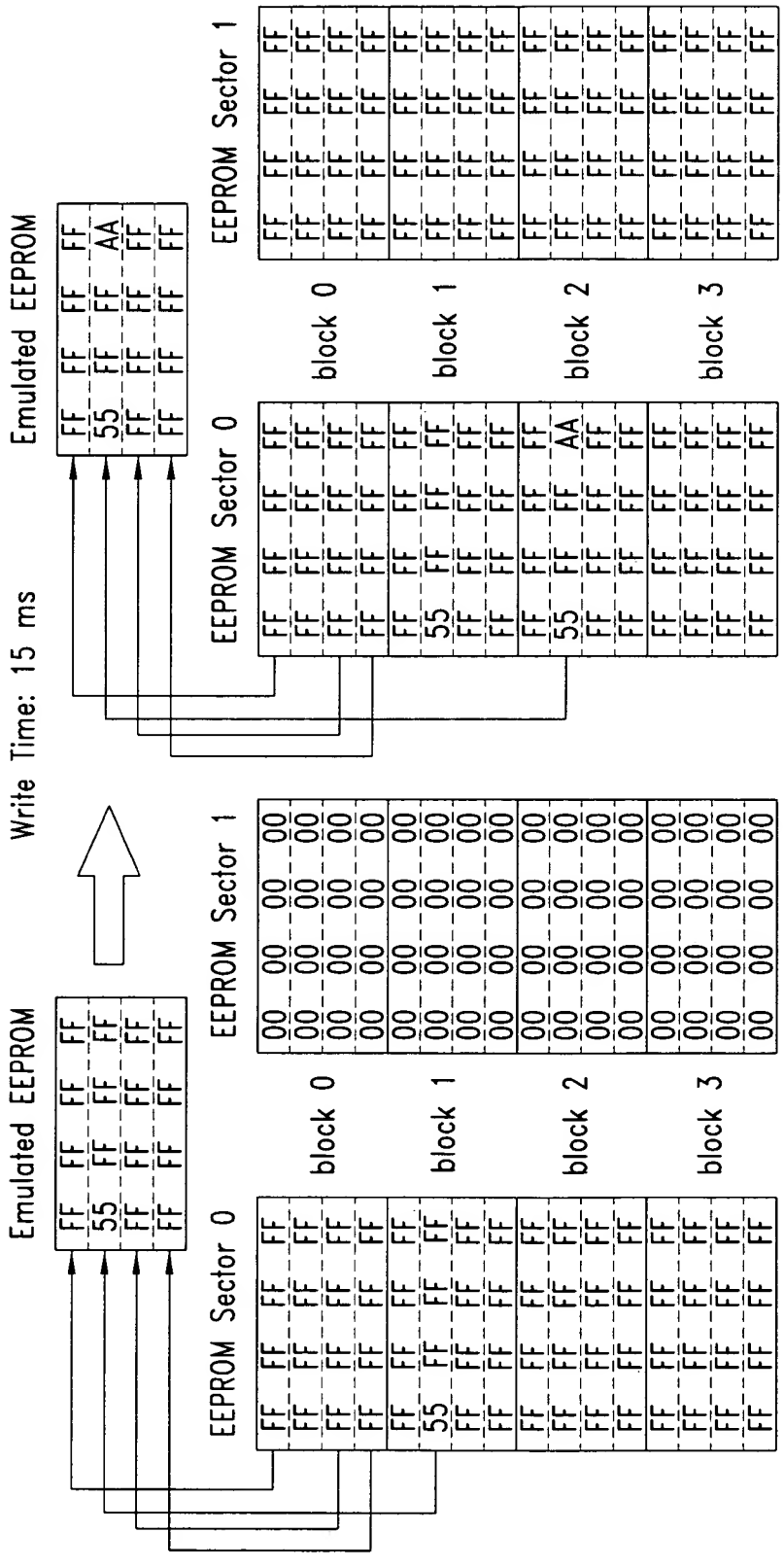
Emulated EEPROM
Write Time: 15 ms
EEPROM Sector 0
EEPROM Sector 1
block 0
block 1
block 2
block 3

*FIG. 6*

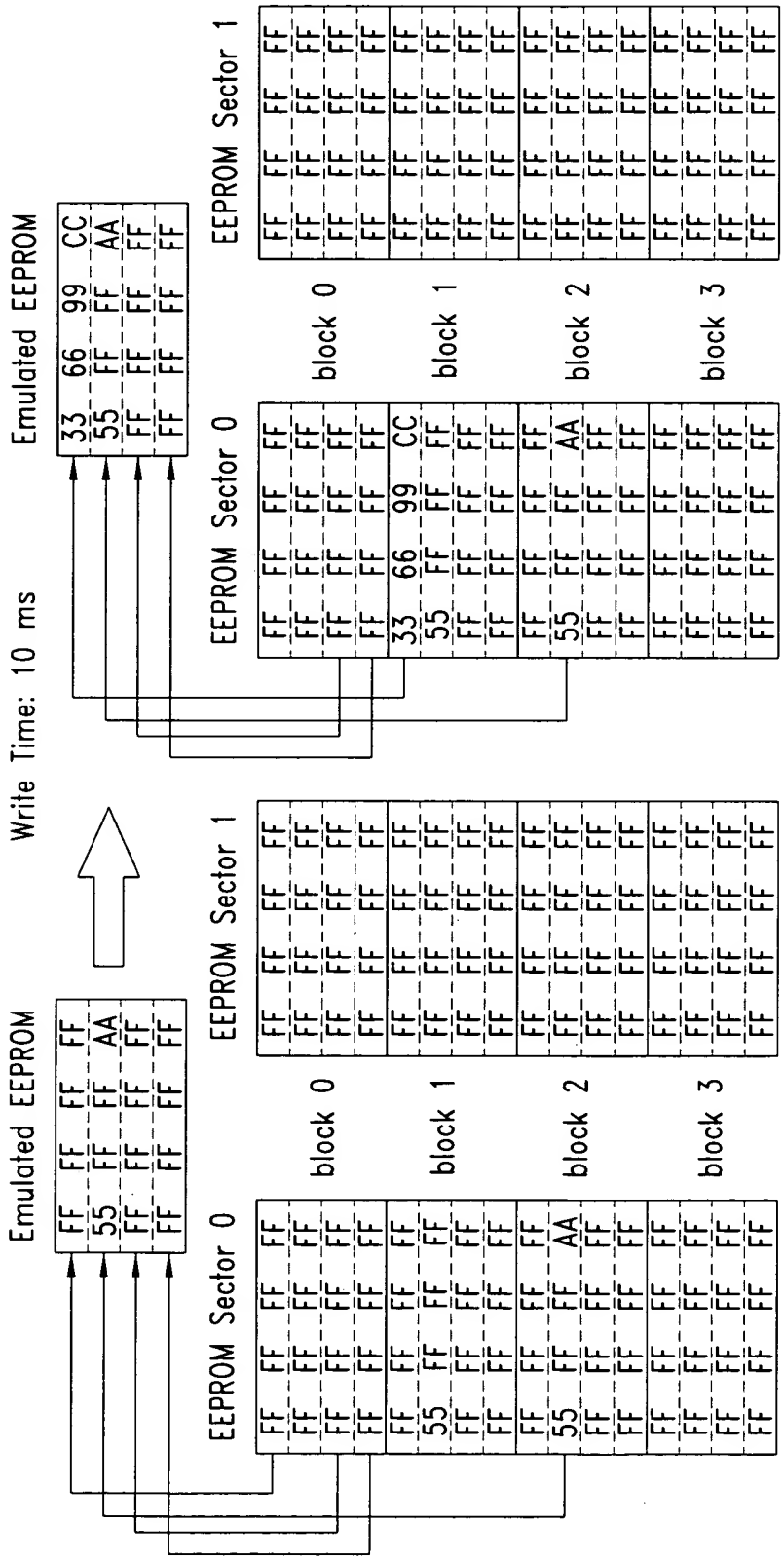
Emulated EEPROM
FF FF FF FF
55 FF FF AA
FF FF FF FF
FF FF FF FF
Write Time: 10 ms
EEPROM Sector 0
EEPROM Sector 1
block 0
block 1
block 2
block 3
Emulated EEPROM
33 66 99 CC
55 FF FF AA
FF FF FF FF
FF FF FF FF

*FIG. 7*

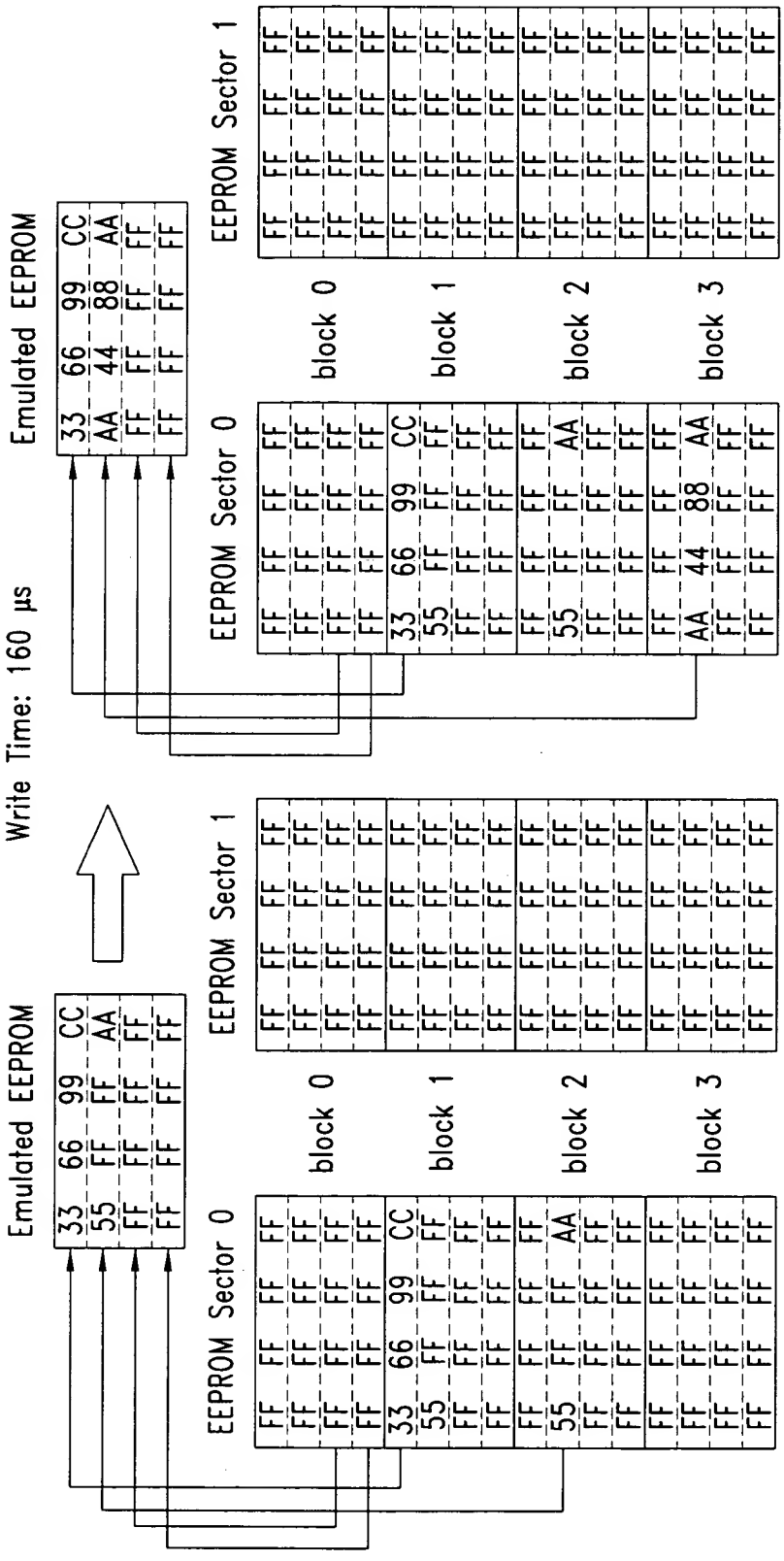
Emulated EEPROM
33 66 99 CC
55 FF FF AA
FF FF FF FF
FF FF FF FF
Write Time: 160 µs
EEPROM Sector 0
EEPROM Sector 1
block 0
block 1
block 2
block 3
Emulated EEPROM
33 66 99 CC
AA 44 88 AA
FF FF FF FF
FF FF FF FF

*FIG. 8*

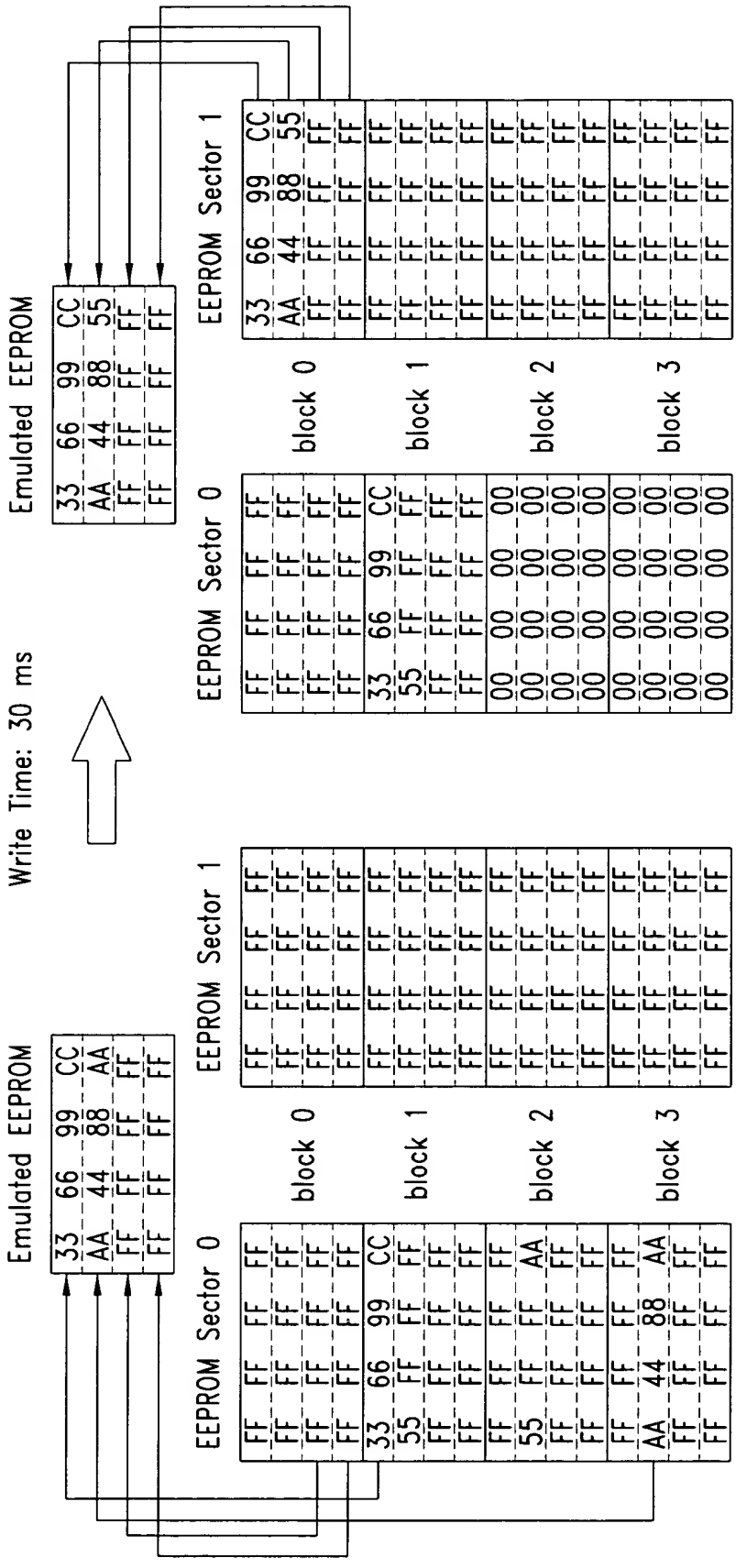
Emulated EEPROM
33 66 99 CC
AA 44 88 55
FF FF FF FF
FF FF FF FF
EEPROM Sector 1
EEPROM Sector 0
block 0
block 1
block 2
block 3
Write Time: 30 ms
Emulated EEPROM
33 66 99 CC
AA 44 88 AA
FF FF FF FF
FF FF FF FF
EEPROM Sector 0
EEPROM Sector 1
block 0
block 1
block 2
block 3

*FIG. 9*

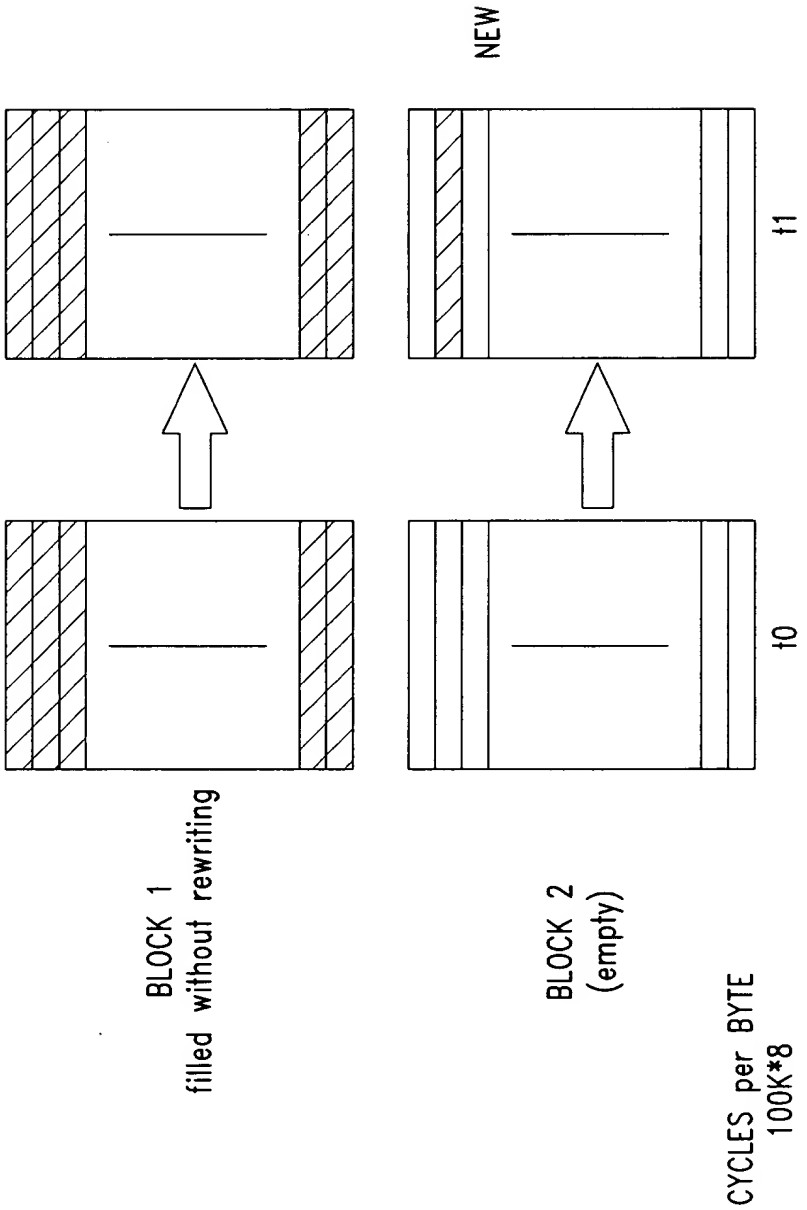
NEW
t1
t0
BLOCK 1
filled without rewriting
BLOCK 2
(empty)
CYCLES per BYTE
100K*8

*FIG. 10*

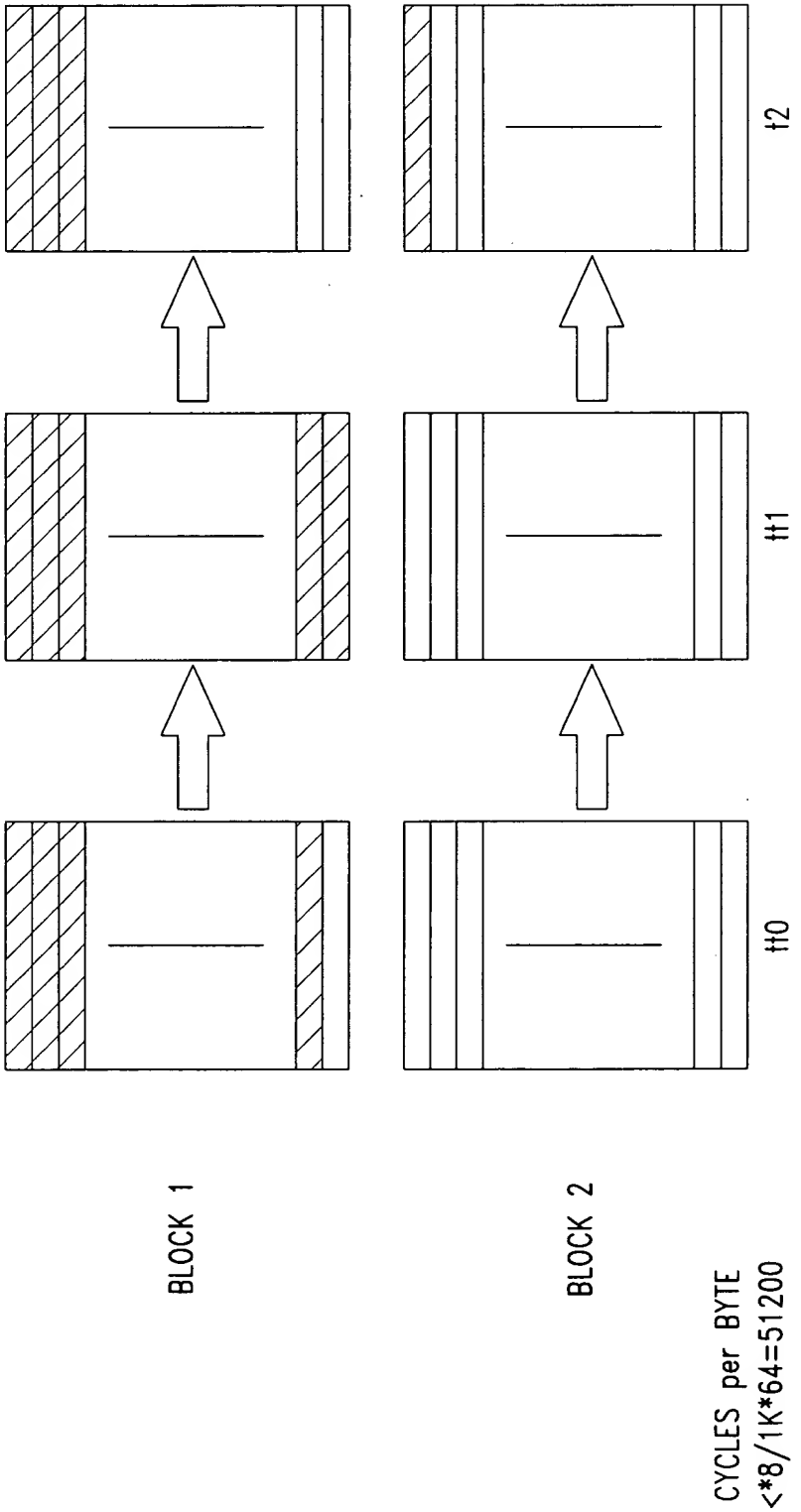


*FIG. 11*

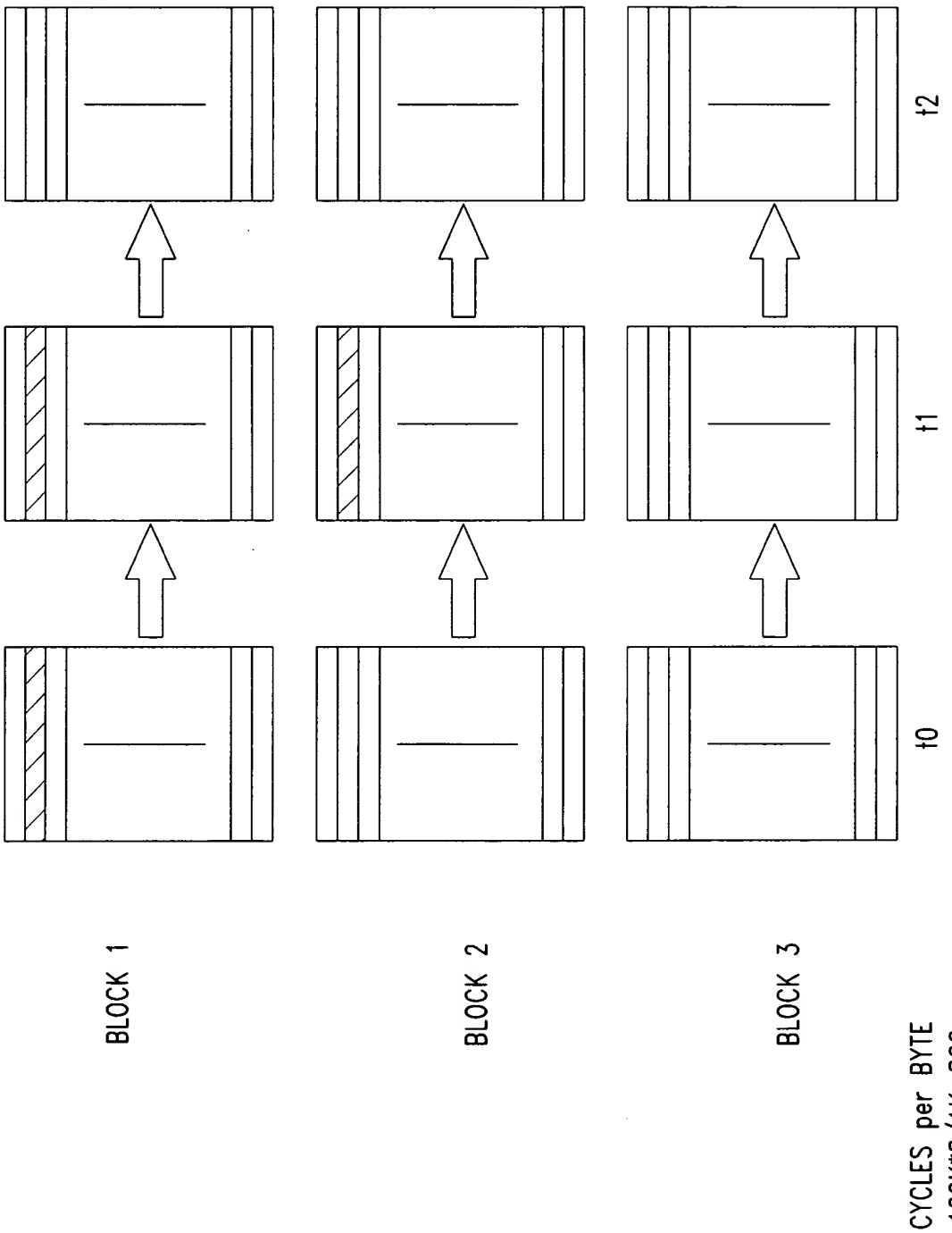


*FIG. 12*

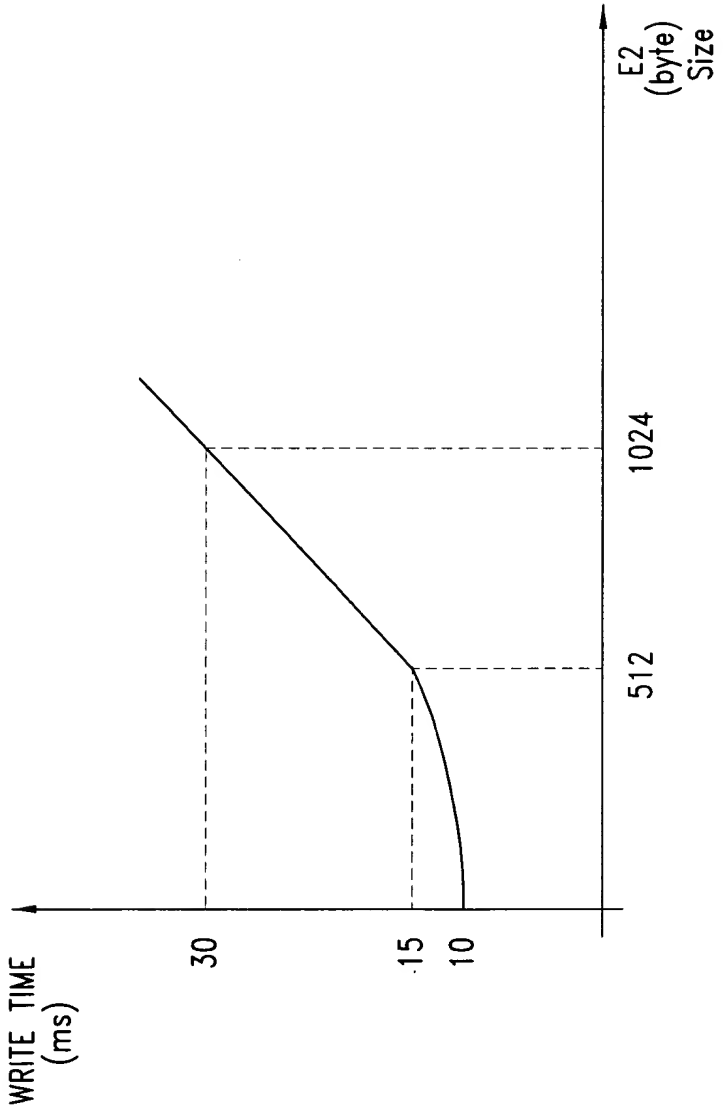


FIG. 13

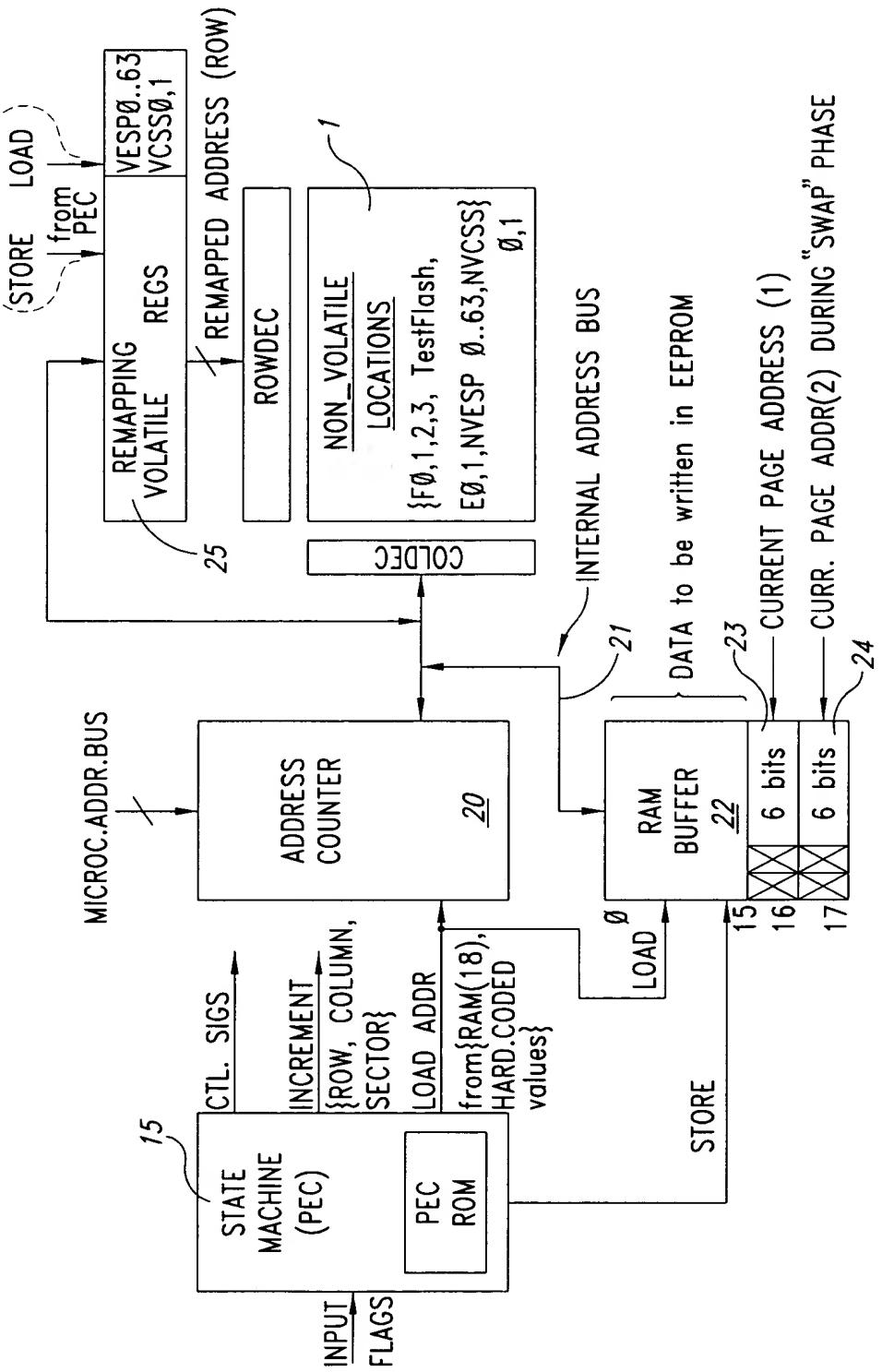
STORE LOAD
from PEC
VESPØ..63
VCSSØ,1
REMAPPING VOLATILE REGS
REMAPPED ADDRESS (ROW)
ROWDEC
NON_VOLATILE LOCATIONS
{FØ,1,2,3, TestFlash,
EØ,1,NVESP Ø..63,NVCSS}
Ø,1
1
25
COLDEC
INTERNAL ADDRESS BUS
21
DATA to be written in EEPROM
23
CURRENT PAGE ADDRESS (1)
CURR. PAGE ADDR(2) DURING "SWAP" PHASE
24
MICROC.ADDR.BUS
ADDRESS COUNTER
20
RAM BUFFER
22
6 bits
6 bits
Ø
LOAD
15
16
17
15
STATE MACHINE (PEC)
PEC ROM
CTL. SIGS
INCREMENT
{ROW, COLUMN, SECTOR}
LOAD ADDR
from{RAM(18), HARD.CODED values}
STORE
INPUT FLAGS

FIG. 14